Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	5375	"718"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/21 07:31
L2	0	l1 and (((cpu or processor or controller) with ((alter$5 or switch$4 or reset$4 or chang$4 or adjust$4) with(speed or frequency or rate)))same ((usage or utilization or utiliz$4)near5 ((exceed$4 or cross$4 or beyond or more or high$3) adj4 (threshold or range or limit or value or reference))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/21 07:30
L3	0	l1 and (((cpu or processor or controller) with ((alter$5 or switch$4 or reset$4 or chang$4 or adjust$4 or throttl$4) with(speed or frequency or rate)))same ((usage or utilization or utiliz$4)near5 ((exceed$4 or cross$4 or beyond or more or high$3) adj4 (threshold or range or limit or value or reference))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/21 07:31
L4	23365	"713"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/21 07:31
L5	4	l4 and (((cpu or processor or controller) with ((alter$5 or switch$4 or reset$4 or chang$4 or adjust$4 or throttl$4) with(speed or frequency or rate)))same ((usage or utilization or utiliz$4)near5 ((exceed$4 or cross$4 or beyond or more or high$3) adj4 (threshold or range or limit or value or reference))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/21 07:43
L6	2	"6470456".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/21 07:44

L7	1	"6470456".uref.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/21 07:44
L8	2	("5778194" | "5832284").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/21 07:44
L9	1	("6470456").URPN.	USPAT	OR	ON	2005/12/21 07:46
L10	28	("4485440" | "5021679" | "5072376" | "5153535" | "5307003" | "5349688" | "5564015" | "5623647" | "5627412" | "5710929" | "5719800" | "5745375" | "5752011" | "5787294" | "5815693" | "5974557" | "5982814" | "6006336" | "6105142" | "6118306" | "6192479" | "6212644" | "6216235" | "6272642" | "6470456" | "6487668" | "6557108" | "6574739").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/21 07:46

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	7	((measur$5 or calculat$4 or determin$5 or detect$4 or estimat$4)with((CPU or processor or controller)near3 (usage or utilization or utility or utiliz$4)))same (((idle adj thread)or registry)near3 (valu$2 or information or number))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/21 08:56

Terms used **clock throttle oh**

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Relevance scale

1 Time Warp simulation on clumps

Girindra D. Sharma, Radharamanan Radhakrishnan, Umesh Kumar V. Rajasekaran, Nael Abu-Ghazaleh, Philip A. Wilsey

May 1999 **Proceedings of the thirteenth workshop on Parallel and distributed simulation**

Publisher: IEEE Computer Society

Full text available: pdf(648.99 KB) Publisher Site

Additional Information: full citation, abstract, references, citings, index terms

Traditionally, parallel discrete-event simulators based on the Time Warp synchronization protocol have been implemented using either the shared memory programming model or the distributed memory, message passing programming model. This was because the preferred hardware platform was either a shared memory multiprocessor workstation or a network of uniprocessor workstations. However, with the advent of "clumps" (cluster of shared memory multiprocessors), a change in this dichotomous view becomes ...

2 Special section: Reasoning about structure, behavior and function

B. Chandrasekaran, Rob Milne

July 1985 **ACM SIGART Bulletin**, Issue 93

Publisher: ACM Press

Full text available: pdf(5.13 MB)

Additional Information: full citation, abstract, references

The last several years' of work in the area of knowledge-based systems has resulted in a deeper understanding of the potentials of the current generation of ideas, but more importantly, also about their limitations and the need for research both in a broader framework as well as in new directions. The following ideas seem to us to be worthy of note in this connection.

3 A method for mapping an analysis to a reusable design

Kelly L. Spicer, David A. Umphress

October 1991 **ACM SIGAda Ada Letters**, Volume XI Issue 9

Publisher: ACM Press

Full text available: pdf(911.99 KB)

Additional Information: full citation, abstract, index terms

Design reuse has more potential for increasin g the productivity of software development and maintenance than does traditional approaches to software reuse. Current software developmen t methods do not promote design reuse. A design mapping method from an object-oriented requirements analysis to a design adhering to thes e principles is presented. The method involves tw o transformation steps and introduces four representation tools for conducting the transformations. The second step produces Ad ...

Results 1 - 3 of 3

Terms used **clock throttle Lee** Found **7** of **169,166**

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Results 1 - 7 of 7

Relevance scale

1 Advances in accelerated simulation: Circuit-aware architectural simulation

Seokwoo Lee, Shidhartha Das, Valeria Bertacco, Todd Austin, David Blaauw, Trevor Mudge

June 2004 **Proceedings of the 41st annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(291.91 KB) Additional Information: full citation, abstract, references, citings, index terms

Architectural simulation has achieved a prominent role in the system design cycle by providing designers the ability to quickly examine a wide variety of design choices. However, the recent trend in system design toward architectures that react to circuit-level phenomena has outstripped the capabilities of traditional cycle-based architectural simulators. In this paper, we present an architectural simulator design that incorporates a circuit modeling capability, permitting architectural-level si ...

Keywords: architectural simulation, circuit simulation, computer system simulation, high-performance simulation

2 Global Virtual Time and distributed synchronization

Jeffrey S. Steinman, Craig A. Lee, Linda F. Wilson, David M. Nicol

July 1995 **ACM SIGSIM Simulation Digest , Proceedings of the ninth workshop on Parallel and distributed simulation PADS '95**, Volume 25 Issue 1

Publisher: IEEE Computer Society, ACM Press

Full text available: pdf(1.46 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Global Virtual Time (GVT) is the fundamental synchronization concept in optimistic simulations. It is defined as the earliest time tag within the set of unprocessed pending events in distributed simulation. A number of techniques for determining GVT have been proposed in recent years, each having their own intrinsic properties. However, most of these techniques either focus on specific types of simulation problems or assume specific hardware support. This paper specifically addresses the GV ...

Keywords: GVT computation, SPEEDES GVT, SPEEDES framework, Synchronous Parallel Environment for Emulation and Discrete-Event Simulation framework, digital simulation, distributed simulation, distributed synchronization, efficiency, event processing, flow control, fundamental synchronization concept, global reduction operations, global virtual time, interactive support, message passing, optimistic simulations, parallel programming, portability, real time use, real-time systems, scalability, software fault tolerance, synchronisation, unprocessed pending events

3 ISSCC highlights: Design and implementation of the POWER5™ microprocessor

Joachim Clabes, Joshua Friedrich, Mark Sweet, Jack DiLullo, Sam Chu, Donald Plass, James Dawson, Paul Muench, Larry Powell, Michael Floyd, Balaram Sinharoy, Mike Lee, Michael Goulet, James Wagoner, Nicole Schwartz, Steve Runyon, Gary Gorman, Phillip Restle, Ronald Kalla, Joseph McGill, Steve Dodson

June 2004 **Proceedings of the 41st annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(422.45 KB) Additional Information: full citation, abstract, references, index terms

POWER5 offers significantly increased performance over previous POWER designs by incorporating simultaneous multithreading, an enhanced memory subsystem, and extensive RAS and power management support. The 276M transistor processor is implemented in 130nm silicon-on-insulator technology with 8-level of Cu metallization and operates at >1.5 GHz.

Keywords: POWER5, clock gating, microprocessor design, power reduction, simultaneous multi-threading (SMT), temperature sensor

4 Tolerating memory latency through push prefetching for pointer-intensive applications

Chia-Lin Yang, Alvin R. Lebeck, Hung-Wei Tseng, Chien-Hao Lee

December 2004 **ACM Transactions on Architecture and Code Optimization (TACO)**, Volume 1 Issue 4

Publisher: ACM Press

Full text available: pdf(590.24 KB) Additional Information: full citation, abstract, references, index terms

Prefetching is often used to overlap memory latency with computation for array-based applications. However, prefetching for pointer-intensive applications remains a challenge because of the irregular memory access pattern and pointer-chasing problem. In this paper, we proposed a cooperative hardware/software prefetching framework, the push architecture, which is designed specifically for linked data structures. The push architecture exploits program structure for future address generation instea ...

Keywords: Prefetch, linked data structures, memory hierarchy, pointer-chasing

5 The M-Machine multicomputer

Marco Fillo, Stephen W. Keckler, William J. Dally, Nicholas P. Carter, Andrew Chang, Yevgeny Gurevich, Whay S. Lee

December 1995 **Proceedings of the 28th annual international symposium on Microarchitecture**

Publisher: IEEE Computer Society Press

Full text available: pdf(1.29 MB) Additional Information: full citation, references, citings, index terms

6 High Efficiency Counter Mode Security Architecture via Prediction and Precomputation

Weidong Shi, Hsien-Hsin S. Lee, Mrinmoy Ghosh, Chenghuai Lu, Alexandra Boldyreva

June 2005 **Proceedings of the 32nd Annual International Symposium on Computer Architecture ISCA '05**

Publisher: IEEE Computer Society

Full text available: pdf(1.37 MB) Additional Information: full citation, abstract

Encrypting data in unprotected memory has gained much interest lately for digital rights protection and security reasons. Counter Mode is a well-known encryption scheme. It is a symmetric-key encryption scheme based on any block cipher, e.g. AES. The schemeýs encryption algorithm uses a block cipher, a secret key and a counter (or a sequence number) to generate an encryption pad which is XORed with the data stored in memory. Like other memory encryption schemes, this method suffers from the inhe ...

7 Avoiding conflict misses dynamically in large direct-mapped caches

Brian N. Bershad, Dennis Lee, Theodore H. Romer, J. Bradley Chen

November 1994 **ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proceedings of the sixth international conference on Architectural support for programming languages and operating systems ASPLOS-VI**, Volume 29 , 28 Issue 11 , 5

Publisher: ACM Press

This paper describes a method for improving the performance of a large direct-mapped cache by reducing the number of conflict misses. Our solution consists of two components: an inexpensive hardware device called a Cache Miss Lookaside (CML) buffer that detects conflicts by recording and summarizing a history of cache misses, and a software policy within the operating system's virtual memory system that removes conflicts by dynamically remapping pages whenever large numbers of conflict miss ...

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Terms used **clock throttle cpu usage** Found **5** of **169,166**

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1 Session 3: Energy-aware OS's: The benefits of event: driven energy accounting in power-sensitive systems

Frank Bellosa

September 2000 **Proceedings of the 9th workshop on ACM SIGOPS European workshop: beyond the PC: new challenges for the operating system**

Publisher: ACM Press

Full text available: pdf(86.80 KB) Additional Information: full citation, abstract, references, citings

A prerequisite of energy-aware scheduling is precise knowledge of any activity inside the computer system. Embedded hardware monitors (e.g., processor performance counters) have proved to offer valuable information in the field of performance analysis. The same approach can be applied to investigate the energy usage patterns of individual threads. We use information about active hardware units (e.g., integer/floating-point unit, cache/memory interface) gathered by event counters to establish a t ...

2 Mitigating Amdahl's Law through EPI Throttling

Murali Annavaram, Ed Grochowski, John Shen

May 2005 **ACM SIGARCH Computer Architecture News , Proceedings of the 32nd Annual International Symposium on Computer Architecture ISCA '05**, Volume 33 Issue 2

Publisher: IEEE Computer Society, ACM Press

Full text available: pdf(202.69 KB) Additional Information: full citation, abstract

This paper is motivated by three recent trends in computer design. First, chip multiprocessors (CMPs) with increasing numbers of CPU cores per chip are becoming common. Second, multi-threaded software that can take advantage of CMPs will soon become prevalent. Due to the nature of the algorithms, these multi-threaded programs inherently will have phases of sequential execution; Amdahlýs law dictates that the speedup of such parallel programs will be limited by the sequential portion of the comp ...

3 Power management and voltage scaling: Runtime identification of microprocessor energy saving opportunities

W. L. Bircher, M. Valluri, J. Law, L. K. John

August 2005 **Proceedings of the 2005 international symposium on Low power electronics and design ISLPED '05**

Publisher: ACM Press

Full text available: pdf(244.51 KB) Additional Information: full citation, abstract, references, index terms

High power consumption and low energy efficiency have become significant impediments to future performance improvements in modern microprocessors. This paper contributes to the solution of these problems by presenting: linear regression models for power consumption and a detailed study of energy efficiency in a modern out-of-order superscalar microprocessor. These simple (2-input) yet accurate (2.6% error) models

provide a valuable tool for identifying opportunities to apply power saving techniq ...

Keywords: energy efficiency, modeling, power, speculative microprocessors

4 Low-power: Critical power slope: understanding the runtime effects of frequency scaling

Akihiko Miyoshi, Charles Lefurgy, Eric Van Hensbergen, Ram Rajamony, Raj Rajkumar
June 2002 **Proceedings of the 16th international conference on Supercomputing**
Publisher: ACM Press

Full text available: pdf(246.89 KB) Additional Information: full citation, abstract, references, citings, index terms

Energy efficiency is becoming an increasingly important feature for both mobile and high-performance server systems. Most processors designed today include power management features that provide processor operating points which can be used in power management algorithms. However, existing power management algorithms implicitly assume that lower performance points are more energy efficient than higher performance points. Our empirical observations indicate that for many systems, this assumption i ...

Keywords: energy aware computing

5 Profile-driven code execution for low power dissipation (poster session)

Diana Marculescu
August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**
Publisher: ACM Press

Full text available: pdf(107.89 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper proposes a novel technique for power-performance trade-off based on profile-driven code execution. Specifically, we show that there is an optimal level of parallelism for energy consumption and propose a compiler-assisted technique for code annotation that can be used at run-time to adaptively trade-off power and performance. As shown by experimental results, our approach is up to 23% better than clock throttling and is as efficient as voltage scaling (up to 10% better in some ca ...

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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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Please edit your search criteria and try again. Refer to the Help pages if you need assistance revising your search.